M.Sc. Semester-III Examination, 2021
UNIVERSITY OF CALCUTTA
ELECTRONIC SCIENCE
Paper Code (CBCC B): ELCGE31
Paper Name: Electronics
Full Marks: 50
Total Time – 2 Hours

INSTRUCTIONS TO THE EXAMINEE

(A) Use blank white paper sheets to write down the answers in your own hand writing. Note that no computer-typed answer scripts will be considered for evaluation.

(B) Write down the following on the first page of your answer scripts:

M.Sc. Semester-III Examination, 2021
Roll No.:-
Registration No.:-
Date of Examination:-
Paper/Course Code:- ELCGE31
Paper/Course Name:- Electronics
Total no. of pages used (including this page):-

(C) You must write your roll number and page no. on the top margin of each page of your answer scripts.

(D) Write your answers mentioning the appropriate question no. starting from the second page onward.

(E) After completion of the examination **at 2:00 pm**, submit the scanned copies or images of all the pages of your answer scripts making "preferably a **single pdf** file or images in **jpeg** format" in digital mode via e-mail **within 2:20 pm**.

(F) File name of your answer scripts should preferably be: XXYY.pdf/jpg and submit your answer scripts to the following e-mail ids: **abhijit_mallik1965@yahoo.co.in, scelc@caluniv.ac.in, akelc@caluniv.ac.in, jselc@caluniv.ac.in with a copy to your Head/Principal**.

Note-1: XX is the abbreviation of your Department/College name.
YY is the last two digits of your roll no.
XX is PH for students of the Department of Physics, CU
XX is AM for students of the Department of Applied Mathematics, CU
XX is GC for students of the Gurudas College

Note-2:

Question Paper Upload Time:	11:50 AM
Examination Start Time:	12:00 Noon
Examination End Time:	2:00 PM
Answer Scripts Submission Time:	2:20 PM

You must follow and abide by these above-mentioned instructions and timing.

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Answer any ***five*** questions

1. (a) Explain the following terms: (i) Compensated semiconductor, (ii) Degenerate semiconductor, and (iii) Minority carrier lifetime. How does the minority carrier lifetime depend on the majority carrier concentration?

   (b) What do you mean by direct and indirect band gap semiconductors? Which one of them favours light emission and why?

   (c) Where does the Fermi level lie for an intrinsic silicon? Justify your answer. (4+3+3)

2. (a) Two different p-n junction diodes are formed- one with silicon and the other with germanium - which one will have higher reverse saturation current and why?

   (b) What do you mean by a linearly graded junction? Show a sketch of charge distribution and electric field distribution in the junction area of such a junction.

   (c) What will happen to the reverse saturation current and junction potential if the temperature of the junction is increased?

   (d) Calculate the contact potential for a p-n junction with $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{16}$ cm^{-3} at room temperature. Given: kT/q = 25.9 meV and $n_i = 9.65 \times 10^9$ cm^{-3} at room temperature, where the terms have their usual meanings.

   (e) What do you mean by destructive and non-destructive breakdowns? What is Zener breakdown? (2+2+2+2+2)

3. (a) Define the (i) emitter injection ratio or emitter efficiency, and (ii) base transportation factor of a transistor.

   (b) What is Early effect of a transistor? How can it account for the input characteristics of a transistor in CB mode?

   (c) Why does the collector current remain practically constant in the active region of the output characteristics of a transistor?

   (d) What are I_{CBO} and I_{CEO}? Give the relationship between them. How does I_{CBO} vary with temperature?

(e) A npn transistor with $\alpha = 0.96$ and negligible I_{CO} carries a base current of 0.2 mA in the active region. Determine the emitter and collector currents. (2+2+2+2+2)

4. (a) Explain why biasing and bias stabilization are needed in a transistor circuit? What is meant by "thermal runaway" of a transistor? How can "thermal runaway" be avoided in a transistor circuit?

(b) Draw the r_e -model of a transistor operating in CE mode. Explain how this model can be established.

c) In the small-signal transistor amplifier of Fig. Q4, $h_{ie} = 560\ \Omega$, $h_{fe} = 100$; h_{re} and h_{oe} are negligible. Draw the *h*-parameter equivalent circuit for the amplifier and determine: (i) Z_i (iii) Z_o and (iii) A_v . (4+3+3)

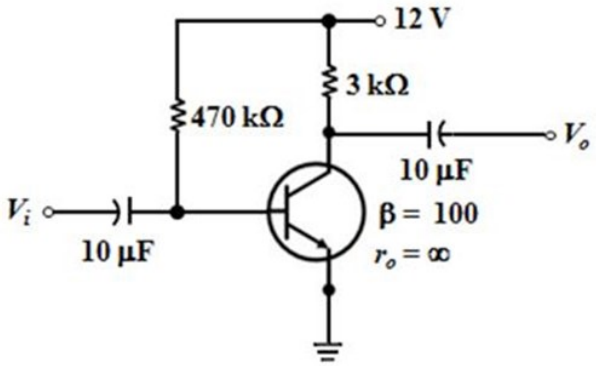

Fig. Q4.

5. (a) Draw the band structure of a metal-oxide-semiconductor (MOS) capacitor under equilibrium condition. With the help of such band diagram explain how the condition for depletion and inversion occurs in a MOS capacitor for biasing and plot the relevant capacitance-voltage characteristics.

(b) With the help of appropriate diagram explain how pinch off occurs in a JFET. How does the current flow from source to drain under such condition? ((2+4+1)+3)

6. (a) Draw the band diagram of a MOSFET from source to drain under the application of both the gate bias and source-to-drain bias. Write down the assumptions of charge sheet model and estimate the amount of inversion charge in the channel of a MOSFET. Define threshold voltage of a MOSFET and explain how this can be measured.

(b) How can be the performance of a MOSFET be improved? Explain the limit of sub-threshold swing of a conventional MOSFET. ((1+4+2)+3)

7. (a) Define sensitivity in a negative feedback amplifier. How is phase distortion reduced by negative feedback?

(b) How is an op-amp used as a logarithmic amplifier?

(c) What is "virtual ground" in an op-amp circuit? ((2+3)+3+2)

8. (a) Simplify the following using a Karnaugh Map:

$$F = \bar{A}\,B + \bar{A}\,C + B\,C + A\,\bar{B}\,C$$

(b) Explain the addition operation 101 + 111 using two full - adders and one half - adder circuit.

(c) Draw the circuit diagram of an encoder and decoder. Explain their operation. (2+2+(3+3))
